IN THE CLAIMS:

1 – 22. (canceled)

23. (new) A microprocessor comprising:

a central processing unit fetching and executing instructions;

a graphics processing module processing image data;

an external interface module; and

a plurality of terminals including a clock terminal,

wherein said central processing unit includes a plurality of registers,

wherein said external interface module outputs a control signal for coupling to an external synchronous memory,

wherein said central processing unit is operable to access said external interface module for accessing said external synchronous memory, and

wherein said microprocessor outputs a clock signal via said clock terminal for coupling to said external synchronous memory.

24. (new) A microprocessor according to claim 23,

wherein said graphics processing module is operable to provide three-dimensional image processing.

25. (new) A microprocessor according to claim 23,

wherein said graphics processing module is operable to provide coordinate transformation processing.

26. (new) A microprocessor according to claim 25,

wherein said graphics processing module is operable to provide perspective transformation processing.

27. (new) A microprocessor according to claim 24,

wherein said microprocessor is operable to output data resulting from three-dimensional image processing to an external LCD device via said terminals.

28. (new) A microprocessor according to claim 24, further comprising:

a cache memory,

wherein said cache memory includes an instruction cache module and a data cache module.

wherein said three-dimensional image processing accelerator is operable to provide perspective transformation processing.

36. (new) A microcomputer according to claim 32,

wherein data resulting from three-dimensional image processing is output to an external LCD device via said terminals.

37. (new) A single chip microcomputer comprising:

a central processing unit;

a cache memory having an instruction cache and a data cache and coupled to said central processing unit;

a three-dimensional image processing accelerator;

a direct memory access controller;

an external interface coupled to said central processing unit, said three-dimensional image processing accelerator and said direct memory access controller; and

a plurality of terminals including a clock terminal;

wherein said external interface module outputs a control signal for provision to an external synchronous dynamic memory via said plurality of terminals,

wherein said central processing unit is operable to access said external interface for accessing said external synchronous dynamic memory, and

wherein a clock signal for provision to said external synchronous dynamic memory is output via said clock terminal.

38. (new) A single chip microcomputer comprising:

a central processing unit;

a memory;

a direct memory access controller coupled to said memory and said central processing unit; and

an external bus interface for coupling to an external synchronous dynamic memory from which can be read a plurality of data continuously,

wherein said direct memory access controller includes a first set of registers which identify a first source address and a first destination address, and a second set of registers which identify a second source address and a second destination address,

29. (new) A microprocessor according to claim 24, further comprising:

a direct memory access controller including a first register and a second register,

wherein said first register contains a starting address, and

wherein said second register contains a transfer address.

30. (new) A microprocessor according to claim 28, further comprising:

a direct memory access controller including a plurality of registers,

wherein said plurality of registers of the direct memory access controller include a control register and an address register.

31. (new) A microprocessor according to claim 24, further comprising:

a clock module including a PLL circuit,

wherein said clock module is operable to multiply a frequency by two times or four times.

32. (new) A microcomputer formed on a single semiconductor substrate comprising:

a central processing unit;

a three-dimensional image processing accelerator;

a direct memory access controller;

an external interface coupled to said central processing unit, said three-dimensional image processing accelerator and said direct memory access controller; and

a plurality of terminals including a clock terminal,

wherein said external interface outputs a control signal for provision to an external synchronous dynamic memory via said plurality of terminals,

wherein said central processing unit is operable to access said external interface for accessing said external synchronous dynamic memory, and

wherein a clock signal for provision to said external synchronous dynamic memory is output via said clock terminal.

33. (new) A microcomputer according to claim 32,

wherein said three-dimensional image processing accelerator includes a divider.

34. (new) A microcomputer according to claim 32,

wherein said microcomputer is operable to provide coordinate transformation processing.

35. (new) A microcomputer according to claim 32,

wherein said direct memory access controller is operable to transfer data between said external synchronous dynamic memory and said memory.

39. (new) A single chip microcomputer comprising:

a central processing unit;

a peripheral module;

a direct memory access controller coupled to said peripheral module and said central processing unit; and

an external bus interface for coupling to an external synchronous dynamic memory with a plurality of memory banks;

wherein said direct memory access controller includes a first register for storing a source address, a second register for storing a destination address, and a third register for storing control information,

wherein said peripheral module is operable to output a transfer request to said direct memory access controller, and

wherein said direct memory access controller is operable to transfer data between said external synchronous dynamic memory and said peripheral module.

40. (new) A single chip microcomputer according to claim 39, further comprising:

a three-dimensional image processing accelerator coupled to said central processing unit,

wherein said external bus interface is operable to output image data processed by said three-dimensional image processing accelerator to said external synchronous dynamic memory.

41. (new) A single chip microcomputer including a clock module having a PLL circuit, wherein said clock module is operable to multiply a frequency by two times or four times, comprising:

a central processing unit;

a three-dimensional image processing accelerator;

a direct memory access controller;

an external interface coupled to said central processing unit, said three dimensional image processing accelerator and said direct memory access controller; and

a plurality of terminals including a clock terminal,

wherein said external interface outputs a control signal to provide to an external synchronous dynamic memory via said plurality of terminals,

wherein said central processing unit is operable to access said external interface for accessing said external synchronous dynamic memory; and

wherein a clock signal for provision to said external synchronous dynamic memory is output via said clock terminal.